UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/664,349	09/17/2003	James F. Caffrey	G0631.70039 US00	4151

7590 01/26/2006

Steven J. Henry
Wolf, Greenfield & Sacks, P.C.
600 Atlantic Avenue
Boston, MA 02210

EXAMINER	
GUTIERREZ, ANTHONY	

ART UNIT	PAPER NUMBER
2857	

DATE MAILED: 01/26/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/664,349	CAFFREY ET AL.	
	Examiner	Art Unit	
	Anthony Gutierrez	2857	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-39* is/are rejected.

7)☒ Claim(s) *2,6,7 and 9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 June 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/10/04, 5/20/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. An English translation was not provided for references EP 0338400 and FR 2737923, listed on Form PTO-1449, dated 5/20/05. These two references were therefore not considered.

Drawings

2. The drawings are objected to because they fail to include a flow diagram for the method steps 31-39.

Response to Arguments

3. The Examiner is persuaded that the original election requirement was not proper, as the requirement was regarding specific components of Applicant's claimed invention useable together as demonstrated in box 20 of Figure 1 of Applicant's Drawings. The Examiner's present Office Action treats all pending claims.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-15, 18-21, and 30-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Friedman et al. (United States Patent Application Publication: US 2002/0049551 A1), in view of Manku et al. (United States Patent: US 6,867,665 B2).

As to claims 1, 20, 21, 30, 31, and 39, Friedman et al. discloses a measuring circuit (see Figs 6a and 6b) for determining a characteristic of the impedance of a complex impedance element (element 36) for facilitating characterization of the impedance thereof, comprising: a signal generating circuit for generating an analog stimulus signal of selectable frequency for applying to the complex impedance element (element 128/ DDS which is defined as "direct digital synthesis" in paragraph 0060), a first receiving circuit for receiving an analog response signal from the complex impedance element in response to the stimulus signal, and for outputting a first output signal indicative of the characteristic of the impedance of the complex impedance element for use in characterization of the impedance of the complex impedance element (elements 120, 124, 100, 102, and 104 and linked elements, that flow into microprocessor 60).

Friedman et al. does not specifically disclose that the measuring circuit is implemented on a single chip.

Manku et al., however, teaches that implementing circuitry in a single chip-design provides significant benefits (col. 5, lines 50-57).

It therefore would have been obvious to one of ordinary skill at the time of invention, to implement the measuring circuit disclosed by Friedman et al. in a single-chip design, as suggested by Manku et al., in order to provide the benefits of eliminating cost, reducing power consumption, and obviating the need to drive off

chip impedances which may not accurately match those of the driving devices, as taught by Manku et al.

As to claims 2, 3, and 32, Friedman et al. discloses a measuring circuit as claimed in Claim 2 in which the first receiving circuit is operable for selectively and alternately outputting the first output signal to be indicative of one of the phase shift and the amplitude change of the stimulus signal caused by the complex impedance element (elements 60 and 132/ Amplitude Control to 128).

As to claims 4, and 33, Friedman et al. discloses that the first receiving circuit comprises a selectable first converting circuit for converting the analog response signal from the complex impedance element to a voltage signal suitable for comparison with the stimulus signal (elements 92 and 102).

As to claims 5, and 34, Friedman et al. discloses a measuring circuit as claimed in Claim 4 in which the first converting circuit comprises a selectable first root-mean-square (RMS) to DC voltage converter for converting the analog response signal from the complex impedance element to a DC voltage level corresponding to the RMS voltage value of the analog response signal (elements 122 and 126).

As to claim 6, Friedman et al. discloses that the first receiving circuit comprises a current to voltage converting circuit for converting the analog response signal to an analog voltage signal (88 and 100).

As to claims 7, and 35, Friedman et al. discloses a measuring circuit in which the first receiving circuit comprises a first analog-to-digital converter for converting the analog response signal from the complex impedance element to a digital signal for providing the first output signal as a digital signal (142 or 144).

As to claim 8, Friedman et al. discloses that the first receiving circuit comprises a first storing means for storing the first output signal in digital form (Outputs/EEPROM).

As to claims 9, and 11, Friedman et al. discloses that a calibration circuit is provided for determining a calibration coefficient for calibrating the first receiving circuit, the calibration circuit comprising a coefficient storing means for storing the calibration coefficient (element 60/Phase Setpoint).

As to claim 10, Friedman et al. discloses that a compensating circuit is provided for selectively applying the calibration coefficient to the first output signal for correcting the first output signal for errors introduced to the response signal by the first receiving circuit (114).

As to claims 12, 13, 14, 15, 18, 19, 27, 36, and 38, Friedman et al. discloses the claimed invention except for a second receiving circuit with duplicate components to those addressed above.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to include a second receiving circuit for the sake of signal comparison to the first for improved accuracy, or to mitigate the case in which one of the circuits has a failure, since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. St. Regis Paper Co. v. Bemis Co., 193 USPQ 8 (1977).

6. Claims 22-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Friedman et al. (United States Patent Application Publication: US 2002/0049551 A1), in

view of Manku et al. (United States Patent: US 6,867,665 B2), further in view of Feldman et al. (United States Patent: US 6,295,272 B1).

As to claim 22, the combination of Friedman et al. and Manku et al. provides a measuring circuit that uses a direct digital synthesis (DDS) generator as addressed above.

The references in the combination do not specifically teach what components comprise the generator.

Feldman et al., however, make use of a DDS generator (see Fig. 12) that comprises: a phase accumulator comprising a counter for incrementing or decrementing its count by a frequency determining digital word to or from a predetermined maximum count value in response to each cycle of a clock signal element 49, specifically 132), a phase-to-amplitude converter for converting count values from the phase accumulator to digital words representative of amplitude values of the stimulus signal (element 108), and a digital-to-analog converter for converting the digital words from the phase-to amplitude converter to the stimulus signal (element 112).

The specific DDS in Feldman provides the benefit of getting an adequate amount of amplitude in the subchannel components at a receiver so as to be detectable with an acceptable bit error rate without causing excessive jitter in the high speed data receiver (col. 19, lines 21-27).

It therefore would have been obvious to one of ordinary skill in the art to use a DDS generator consistent the type taught by Feldman et al., in the circuit employed in the combination of Friedman et al. and Manku et al. to provide an adequate signal for

the receiving circuit, with an acceptable bit error rate, without causing excessive jitter, thus providing further control over the detected vibratory responses of the complex impedance element.

As to claims 23-26, Feldman et al. discloses that the phase-to-amplitude converter comprises a look-up table with the digital words representative of the amplitude values of the stimulus signal cross-referenced with count values from zero to the predetermined maximum count value outputted by the phase accumulator (col. 18, lines 39-45).

As to claim 27, Feldman et al. discloses the direct digital synthesis frequency signal generator comprises an adder for summing a phase offset digital word to each count value outputted by the phase accumulator for offsetting the phase of the stimulus signal by a predetermined offset (Fig. 12, Summing Junction).

As to claims 28 and 29, Feldman et al. discloses the phase offset digital word is selectable for selecting the phase offset of the stimulus signal (col. 24., line 50-col. 25, line20).

7. Claims 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Friedman et al. (United States Patent Application Publication: US 2002/0049551 A1), in view of Manku et al. (United States Patent: US 6,867,665 B2), further in view of Goldberger et al. (United States Patent: 5,772,597).

The combination of Friedman et al. and Manku et al. provides a measuring circuit for monitoring ultrasonically tuned blades as addressed above. These blades are

at times used for determining the condition of skin tissue that they contact (Feldman et al. paragraph 0026).

The combination does not specifically teach the use of a temperature sensor.

Goldberger et al. however, teaches using a temperature sensing device on the blade of an electrosurgical tool or scalpel for the purpose of identifying the tissue based on the temperature measurements (col. 4, lines 13-18, and col. 6, lines 45-62).

It therefore would have been obvious to one of ordinary skill in the art at the time of invention, to include a temperature sensor configuration, as taught by Goldberger et al., in the electric scalpel combination of Friedman et al. and Manku et al., in order to more precisely determine the type of tissue in contact with the blade to more accurately determine the condition of the tissue.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

United States Patent Application Publication: US 2002/0103838 A1, to Kelly, teaches reduction of periodic signals in pseudo-random noise produced with direct digital synthesis.

United States Patents

US 6,906,532, to Slates teaches a digital impedance measuring device including sampling and digitizing first and second voltages.

6,161,420 to Dilger et al., teaches a high frequency measuring circuit used in conjunction with a piezoelectric acoustic device.

5,832,412, to Guez, teaches a programmable digital frequency ultrasonic generator that uses direct digital synthesis.

5,805, 871, to Baxter, teaches a method and system for phase-synchronous, flexible frequency clocking and messaging.

5,042,460, to Sakurai et al., teaches an ultrasonic testing device for inhibiting drive when an ultrasonic element is determined to be defective.

4,832,022, to Tjulkov et al., teaches a cryogenic ultrasonic scalpel that includes a temperature sensor on the blade.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anthony Gutierrez whose telephone number is (571) 272-2215. The examiner can normally be reached on Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marc Hoff can be reached on (571) 272-2216. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Anthony Gutierrez
Examiner
Art Unit 2857

AG

AG
1/20/06

MARC S. HOFF
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800